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A SiC Based 3.6kW High Efficiency and High Power Density Totem-pole PFC

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pcim ASIA

电力电子、智能运动、可再生能源
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International Exhibition and Conference
for Power Electronics, Intelligent Motion,
Renewable Energy and Energy Management

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Wolfspeed

...

2013 - 2017

2017 - 2019

2019 - Now



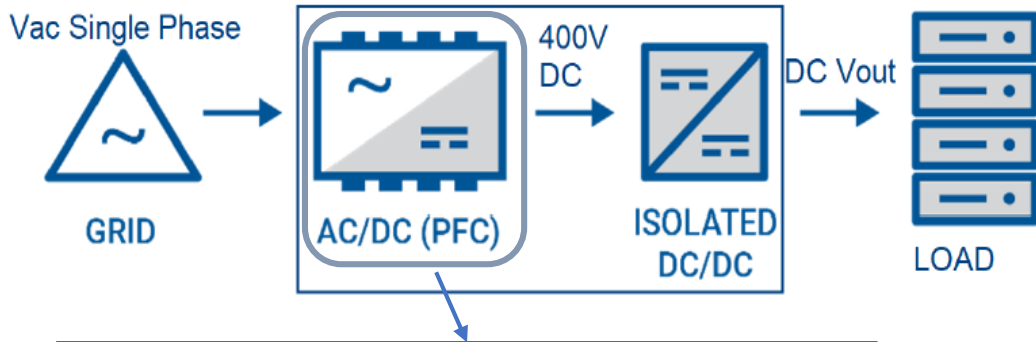
Ying Liu

Ying Liu received the bachelor's degree in electronic engineering from Yanshan University, Hebei, China, in 2017. Ying received the master's degree in power electronics from Harbin Institute of Technology, Shenzhen, China, in 2019.

Ying is generally interested in power electronics, power system, and power semiconductor, together with the applications in various sectors.

Currently, Ying is a senior application engineer of discrete SiC power applications at Wolfspeed China.

Applications – High Efficiency Server Power Supplies

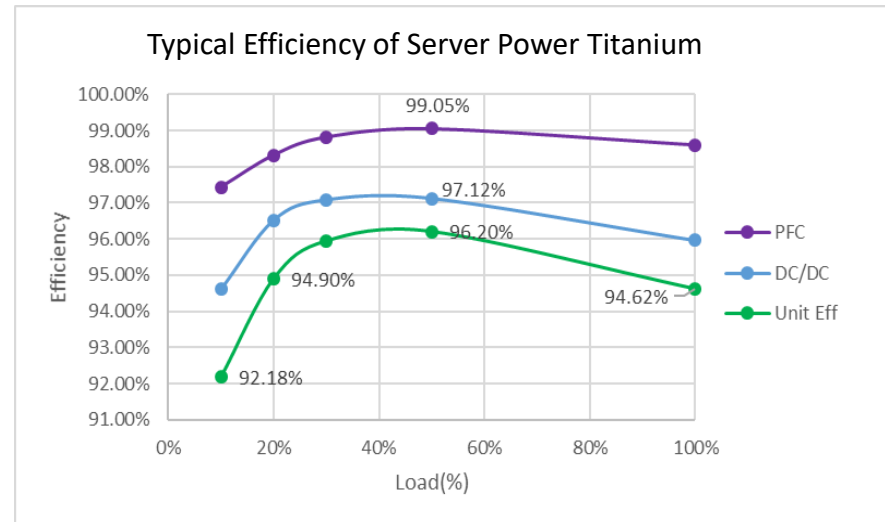


➤ PFC circuit is a critical stage for power factor correction and low total harmonic distortion

Where they are used: Servers, Data centers, Telecom base station, Mining Power, etc.

Trends:

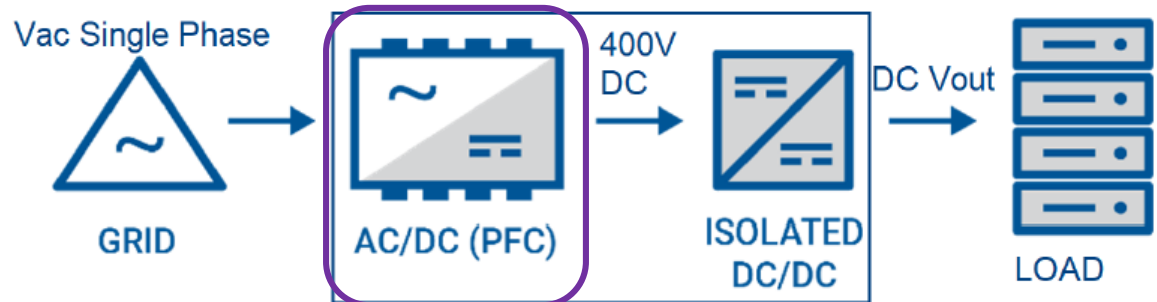
- High efficiency for 80 PLUS® Platinum/Titanium, OCP3.0, High efficiency 5G for Carbon-Neutral
- High power density
- Lower system cost



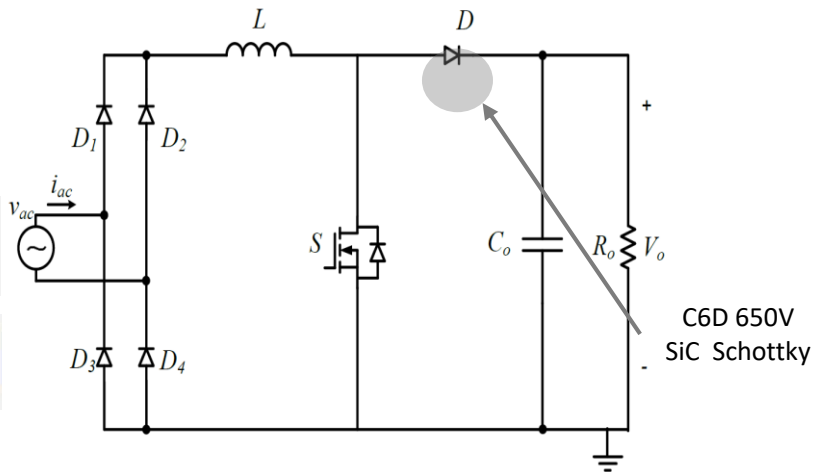
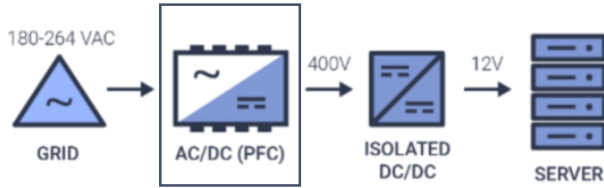
> 99% PFC peak efficiency is required for 80 PLUS Titanium applications

Specification of 3.6kW TT PFC

Parameter	Value	Notes
Input Voltage	180-265 Vac(rms) 230V nominal	Power derating needed for low line
Output Voltage	380 - 400 Vdc	
Output Power	3.6 kW max.	
Switching Frequency f_s	60kHz	
Peak Efficiency η	>99%	With AUX PSU
Silicon Carbide MOSFET	C3M0045065L –HF leg C3M0015065D – LF leg	TOLL package for HF Leg LF can use Si/SiC MOSFET
Form Factor (W x H x L)	73mm x 40mm x 220mm	Power density: 92W/in3

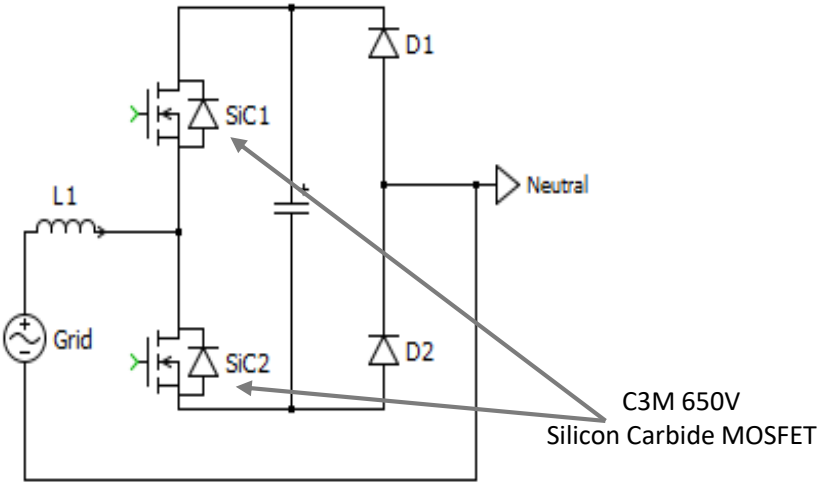


Target PFC Topologies of Server SMPS



Traditional PFC Boost

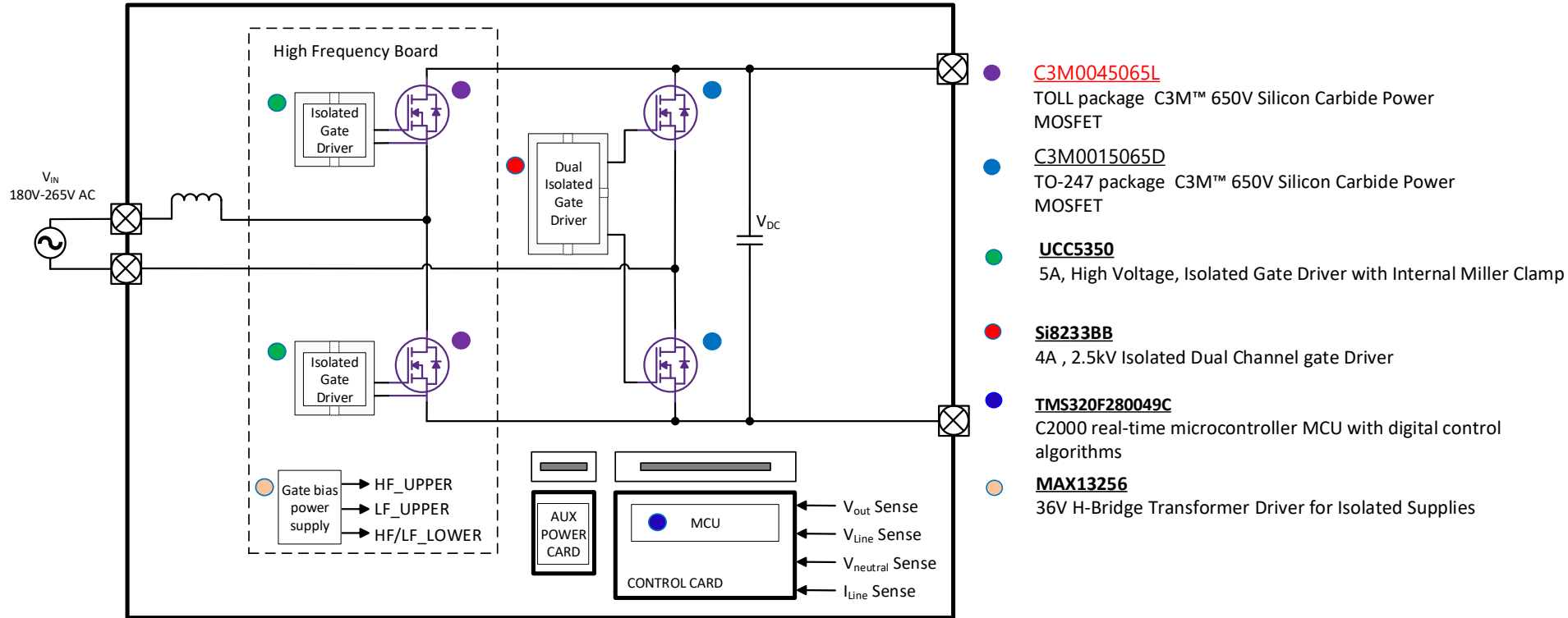
- SiC diode: Low V_f , high reverse blocking voltage, and zero reverse recovery
- Lower 80 PLUS efficiency standards (Silver, Gold)



Bridgeless Totem-Pole PFC

- For HF leg, Si-based MOSFET cannot be used due to slow reverse recovery of body diode
- SiC MOS: Low $R_{ds(on)}$ over Temp, robust body diode and lower switching losses
- 80 PLUS Titanium efficiency standards can be achieved (>99%)

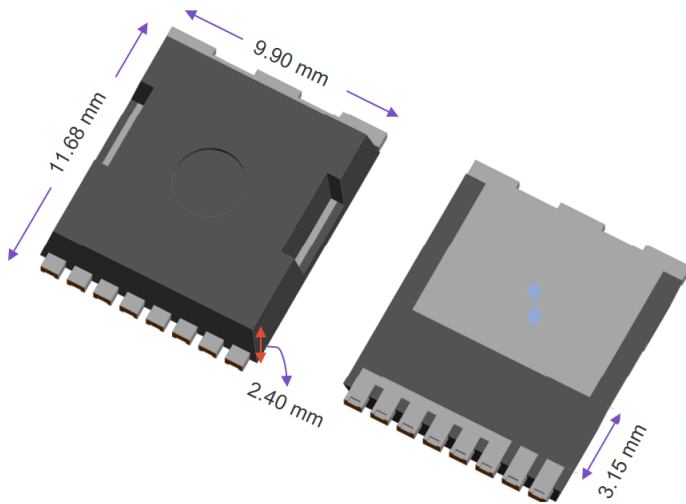
Block Diagram- High Efficiency Design



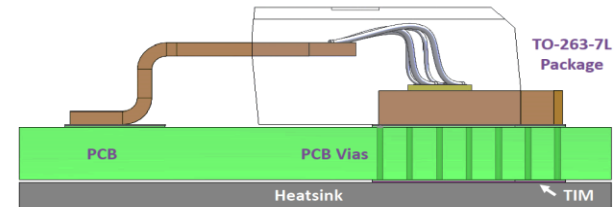
- Daughter cards for high power density and flexibility
- Low-cost low-profile discrete power supply instead of high-cost off-the-shelf ones

Wolfspeed 650 V SiC MOSFET with TOLL (TO Lead-Less) Package

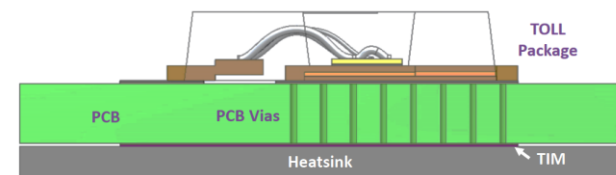
- Low lead inductance enables lower switching losses
- Larger back metal tab enables lower junction temperature
- Ideal for higher switching frequency applications
- 25% smaller footprint as compared to the standard TO-263-7L Package
- Minimum Creepage = 3.15 mm (D-S)
- Ease of automated assembly
- Ideal for ~400VDC applications



New TOLL (TO-Leadless) Package



TO-263-7



TOLL

Parameters and Performance Comparison– PFC Choke

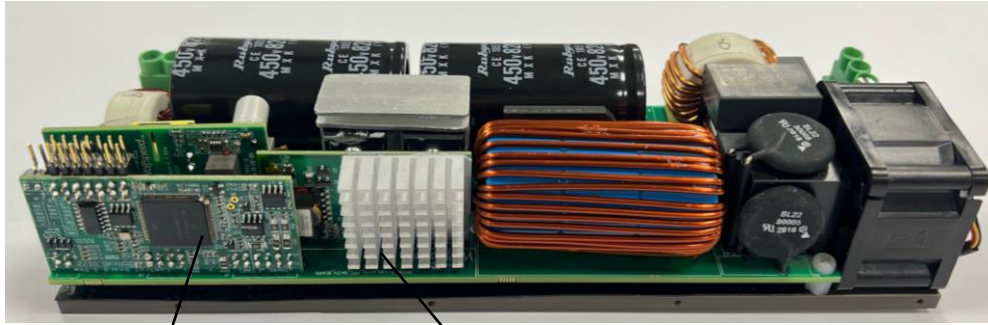
	KH106-060A	KAM106-060A	NPC106060	NPA106060	NPN-LH106060
Permeability	60	60	60	60	60
Pv(100mT @50kHz)	300kW/m ³	200kW/m ³	150kW/m ³	150kW/m ³	200kW/m ³
DC Bias (@100 Oe)	80%	68%	70%	55%	85%
Frequency Range	<200kHz	<200kHz	<200kHz	<300kHz	<200kHz
Vendor	KDM	KDM	POCO	POCO	POCO

- Trade-off between core loss and DC bias
- NPN-LH material selected for its low core loss and best DC bias
- DC bias capability and loss data of POCO can be seen at



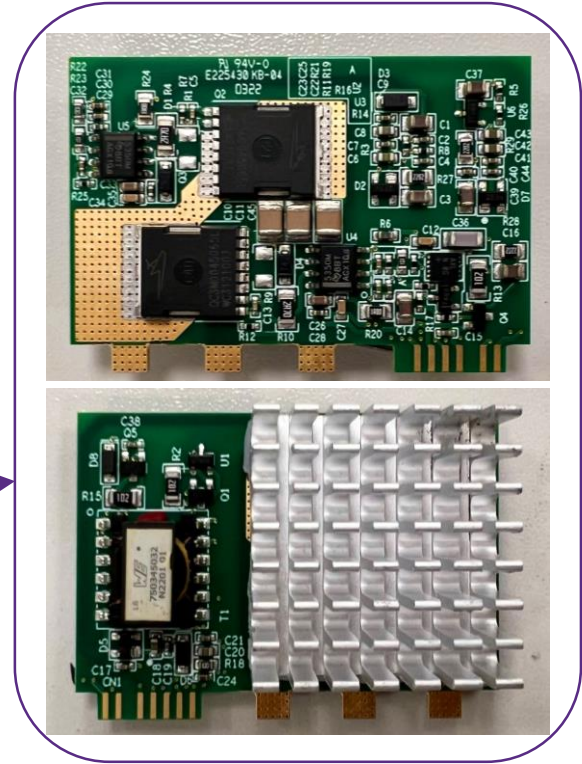
<http://pocomagnetic.com/html/2020/03/02/202003021053158007732711.html>

High-Frequency Half-Bridge Daughter Card (30X45X15mm)



Control card
with TI DSP

Daughter card with SiC
MOSFETs C3M0045065L

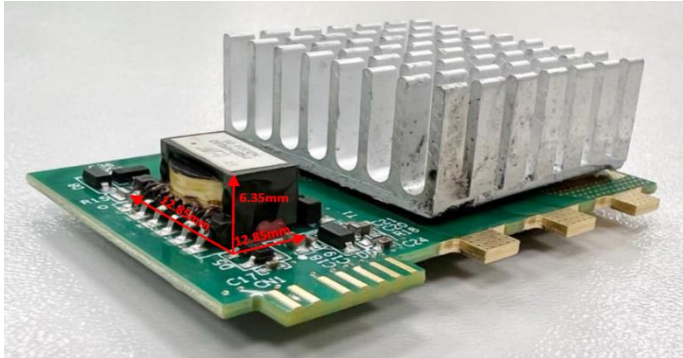


Adhesive(TIA520R) as TIM for
assembling heatsink

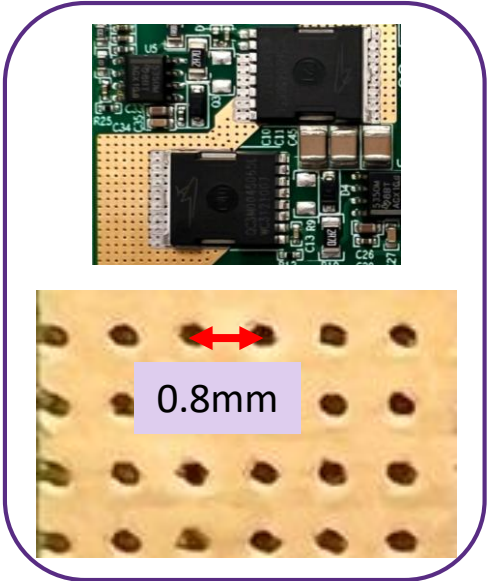
- ❖ Daughter card for high-frequency leg
- ❖ Fully utilize vertical space of power supply
- ❖ Increase power density (saving PCB area)
- ❖ Easy assembly with double-sided edge connectors
- ❖ Quick evaluation of Wolfspeed's Silicon Carbide MOSFETs

- Larger size of heatsink
- One heatsink for HS and LS MOSFET heat dissipation, good to balance the temperature of two MOSFETs
- Additional thermal impedance

High-Frequency Half-Bridge Daughter Card (30X45X15mm)



- Low profile (6.35mm vs. 12.5mm, lower height $\leq 4\text{mm}$ achievable)
- Good for airflow
- SM facilitates automated assembly



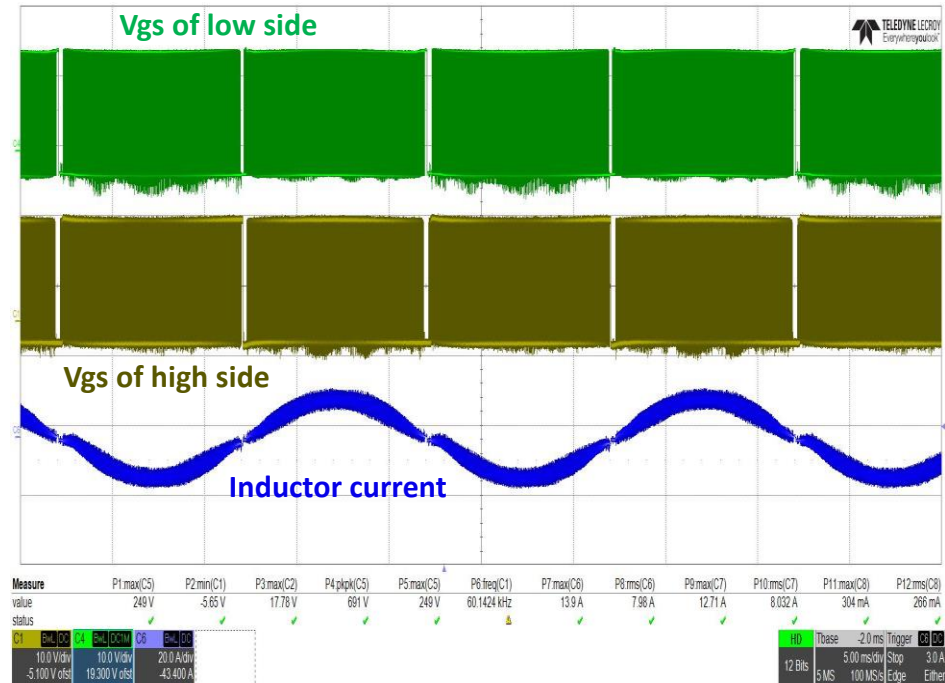
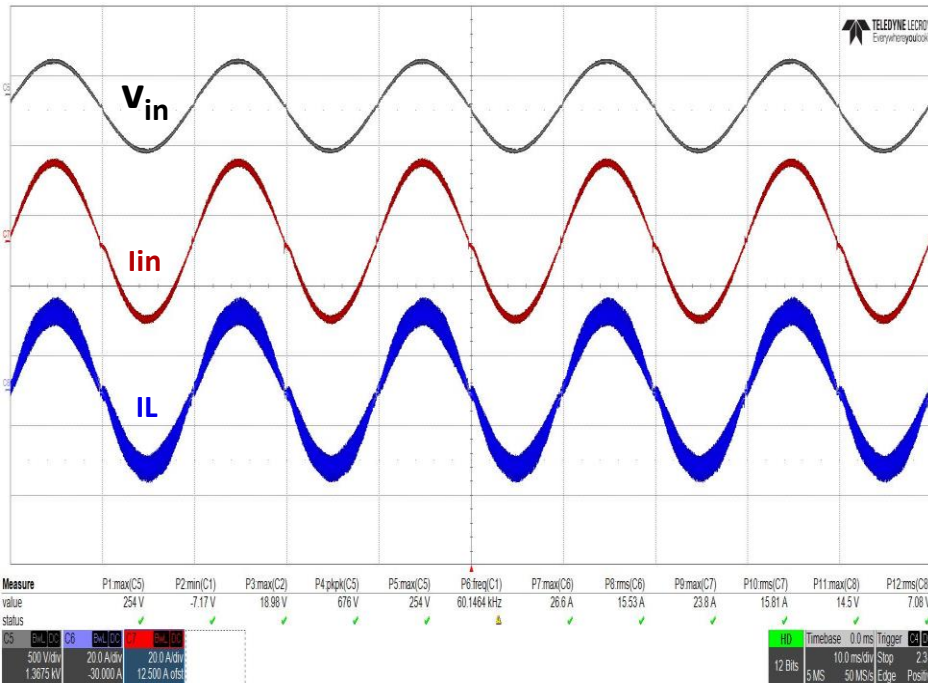
Via spacing: 0.8mm
Via size: 0.4mm with 2.4mil (60 μm) copper plating thickness

Thermal Impedance	Soldering Heatsink	Adhesive TIM	Units
$R_{\theta,JC}$	0.7	0.7	$^{\circ}\text{C}/\text{W}$
$R_{\theta,solder}$	0.015	0.015	$^{\circ}\text{C}/\text{W}$
$R_{\theta,PCB}$	0.45	0.45	$^{\circ}\text{C}/\text{W}$
$R_{\theta,TIM}$	0.03	0.52	$^{\circ}\text{C}/\text{W}$
$R_{\theta,HA}$	5.3	3.4	$^{\circ}\text{C}/\text{W}$
$R_{\theta, total}$	6.5	5.09	$^{\circ}\text{C}/\text{W}$

- Standard PCB manufacture process
- Cost effective

Key waveforms

Test Condition: $V_{in}=230V/50Hz$, $V_o = 400V$, full load



V_{in} : Input voltage [500V/div]

I_{in} : Input current [20A/div]

I_L : Inductor current [20A/div]

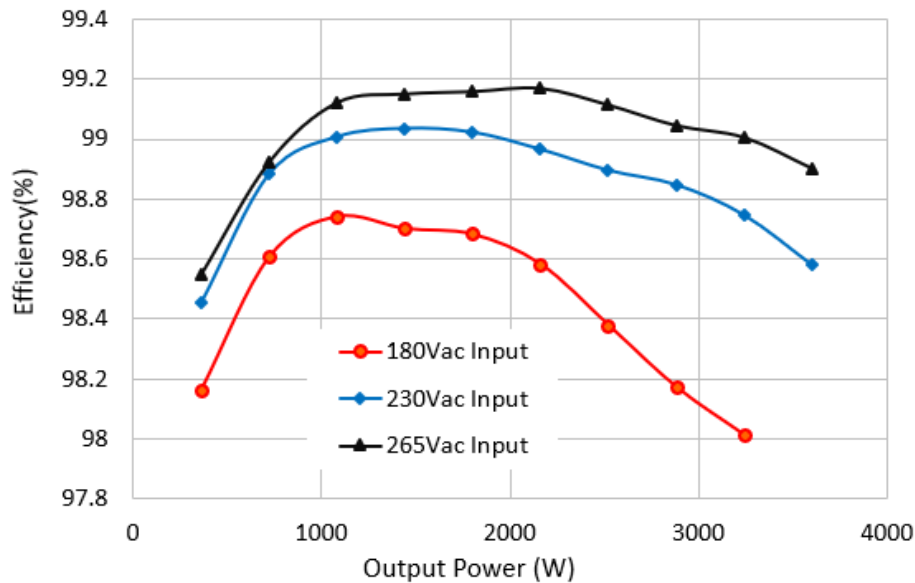
V_{gs} : Vgs of PFC low side [10V/div]

V_{gs} : Vgs of PFC high side [10V/div]

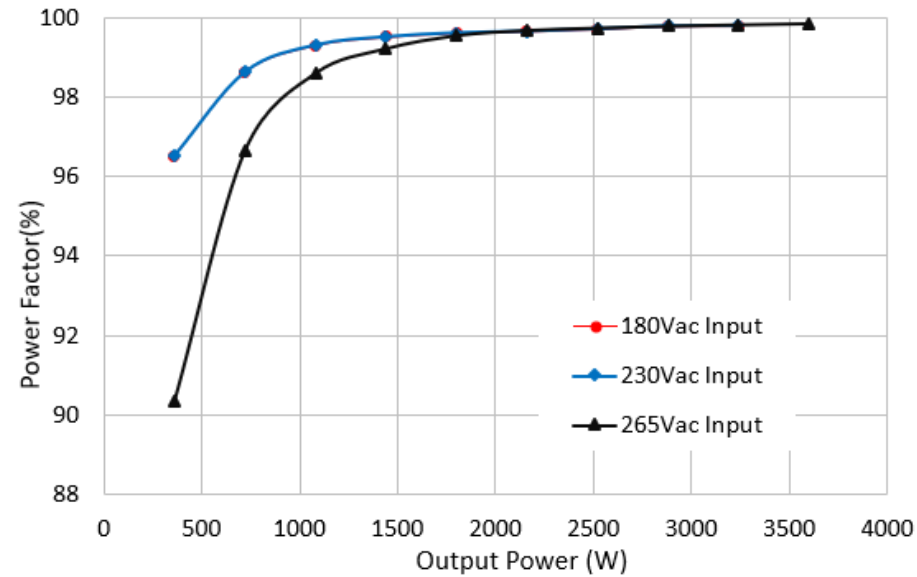
I_L : Inductor current [20A/div]

Efficiency Test results

3.6kW TT PFC Efficiency curve



Power Factor curve



- ✓ Over 99% efficiency achieved at half load even with Aux Power Supply
- ✓ PF > 0.96 at 10% load, PF > 0.99 at half load, PF > 0.995 at full load

Thermal Test Results

	Calculated Power loss (Watts)	Measured Case Temp (°C)	Calculated Junction Temp (°C)	Max. Junction Temperature (°C)	Derating Requirement (°C)	Comments
180Vac Input 400Vdc output 3600W						
High side MOSFET	13.38	82.5	94.27	175	135	Pass
Low side MOSFET	13.38	85	96.77	175	135	Pass
230Vac Input 400Vdc output 3600W (adhesive as TIM)						
High side MOSFET	8.24	63.5	70.75	175	135	Pass
Low side MOSFET	8.24	62	69.25	175	135	Pass

- ✓ SiC MOS with new TOLL package
- ✓ High Efficiency, above 99%
- ✓ High Power Density (92W/in³)



220mmX73mmX40mm